Features

- Transceiver unit with independent
  - 1550nm DFB Laser diode transmitter
  - InGaAs PIN photodiode receiver
- Duplex SC receptacle and plastic package
- +5V Signal power supply, PECL interface logic level
- Operate data rates from 5Mb/s to 700Mb/s (NRZ)
- Long reach SONET/SDH OC-12/STM-4 compliant

Application

- SONET/SDH
- ATM

General

The optical transceiver is a high performance, cost effective module for serial optical data communication applications. It is designed to provide a SONET/SDH compliant link for OC-12/STM-4 long reach links.

Transmitter Section

Transmitter is designed for single mode fiber and operates at a nominal wavelength of 1550nm. The transmitter module uses a DFB laser diode and full IEC825 and CDRH class 1eye safety. It contains APC function, temperature compensation circuit and PECL logic interface, as shown in figure 1.

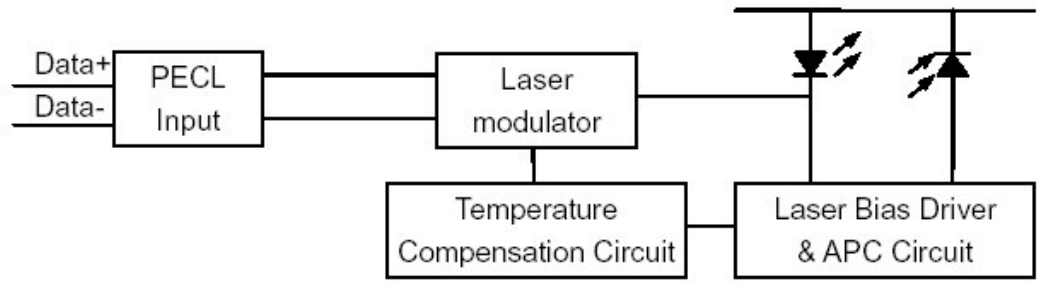


Figure 1. Transmitter Block Diagram

Receiver Section

The receiver section uses a hermetic packaged front and receiver (InGaAs PIN and preamplifier). The postamplifier is ac coupled to preamplifier through a capacitor and a low pass filter, as shown in figure 2. The capacitor and LPF are enough to pass the signal from 5Mb/s to 700Mb/s without significant distortion or performance penalty. The LPF limits the preamplifier bandwidth to improve receiver sensitivity. Figure 2 shows the receiver section, which proves PECL logic differential outputs and a PECL logic signal detect output.

As the input optical is decreased, Signal Detect will switch from high to low (deassert point). As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 0.5dB higher than the de-assert level.

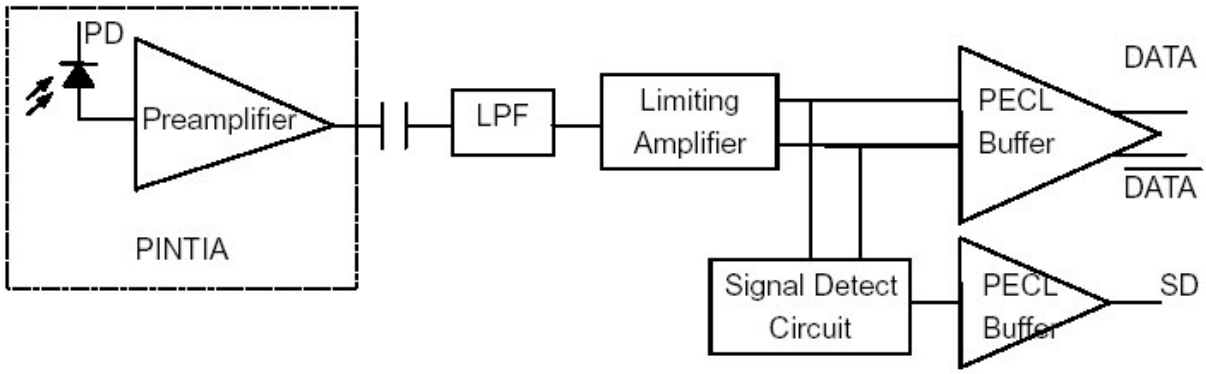


Figure 2. Receiver Block Diagram

Performance Specifications

Table1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-40	+85	℃
Input Voltage	-	GND	Vcc	V
Power Supply Voltage	Vcc-Vee	0	+6	V
Lead Soldering Temperature/Time	-	-	240/10	℃/S
Operating Temperature		0	+70	℃

Note: Stress in excess of maximum absolute ratings can cause permanent damage to the module

Tabel2. Operating Environment

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	+4.75	+5.25	V
Ambient Operating Temperature	-	0	+70	℃

Tabel 3. Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Center Wavelength	λ_p	1480	1550	1580	nm	
Spectral Width	$\Delta\lambda$ (-20dB)	-	-	1	nm	
Average Optical Output Power	Po	-3	-	+2	dBm	
Extinction Ratio	EXT	10	-	-	dB	
Power Supply Current	Icc	-	70	180	mA	1
Output Eye	Compliant with ITU recommendation G.957					
Data Input	PECL					
Receiver						
Parameter	Symbol	Min	Typ	Max	Unit	Note
Sensitivity	Pr	-	-31	-28	dBm	2
Maximum input power	Ps	-3	0	-	dBm	2
Signal Detect Assert Level	-	-45	-	-	dBm	
Signal Detect Deassert Level	-	-	-	-31	dBm	
Signal Detect Hysteresis		-	3	-	dB	
Operating Current	Icc	-	80	120	mA	1
Data Outputs	PECL					
Alarm Output	PECL					

PECL Input Pins SD, TD+ and TD-

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input HIGH voltage	V_{IH}	VCC – 1165	-	VCC - 880	mV	3
Input LOW voltage	V_{IL}	VCC - 1810	-	VCC – 1475	mV	3

PECL Output Pins SD, RD+ and RD-

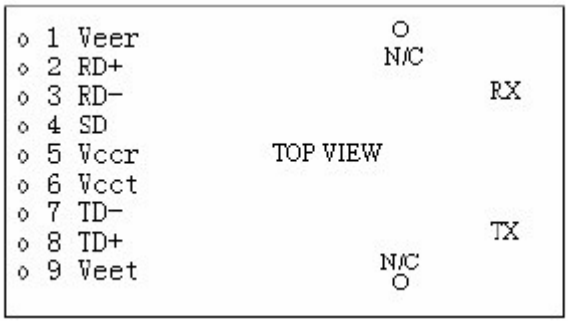
Parameter	Symbol	Min	Typ	Max	Unit	Note
LOW-level output voltage	V_{OL}	VCC – 1840	-	VCC - 1600	mV	3
HIGH-level output voltage	V_{OH}	VCC - 1100	-	VCC – 900	mV	3

Note :

1. **The current excludes the output load current.**
2. **Minimum Sensitivity and saturation levels for a $2^{23}-1$ PRBS with 72 ones and 72 zeros inserted (ITU recommendation G958)**
3. **RL=50R connected to a level of Vcc –2V.**

Pin Definitions

Pin Out Diagram

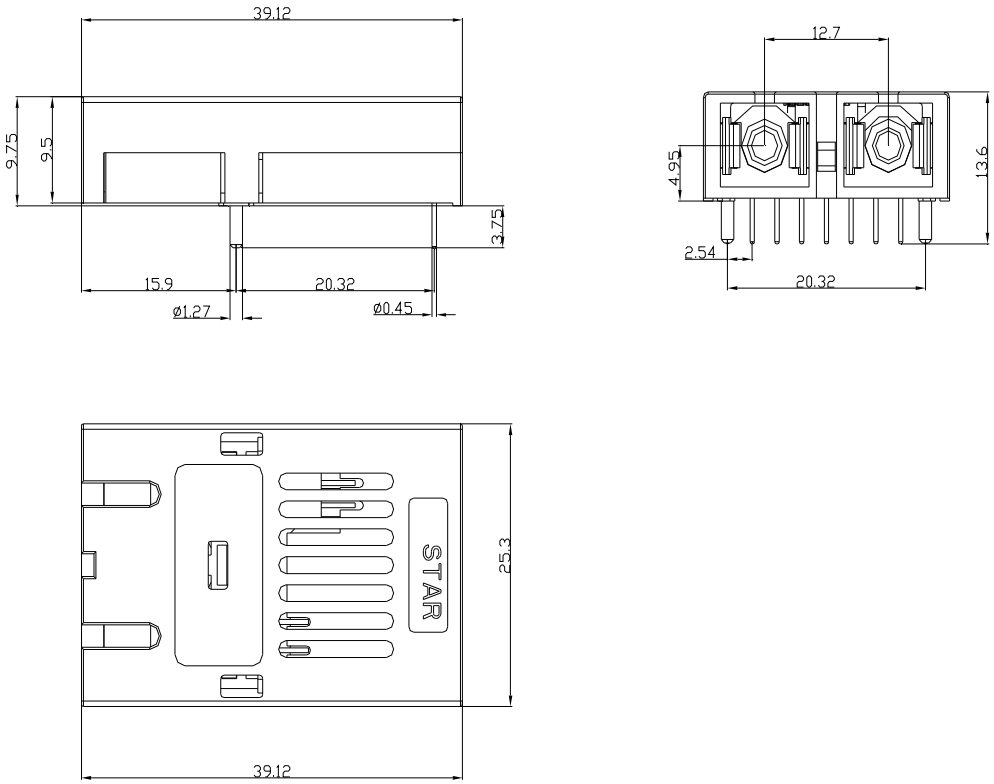


Pin Description

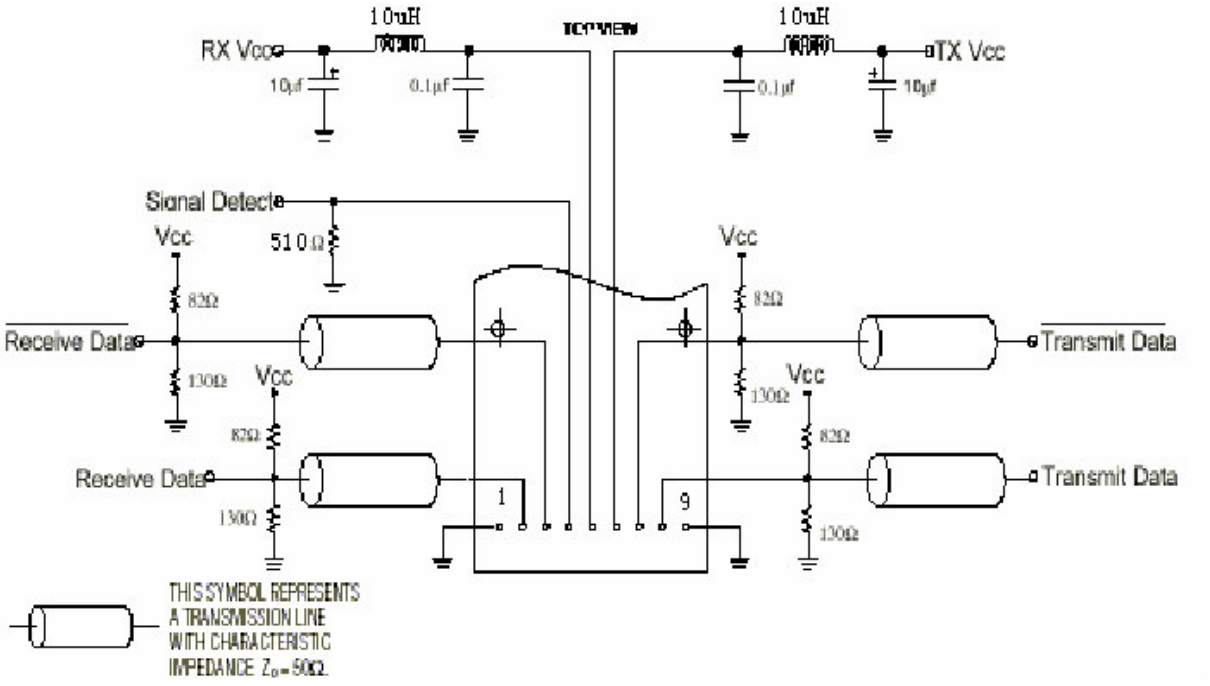
Pin#	Pin Name		Logic Level	Description
N/C	Mounting Studs			The two pins are not connected to the transceiver internal circuit.
1	VEER	RX Ground	N/C	Directly connect this pin to receiver signal ground plane.
2	RD+	RX Output Data	PECL	
3	RD-	RX Output Invert Data	PECL	
4	SD	RX Signal Detect	PECL	Normal Operation: Logic "1" Out put , represents that optical is present at receiver input. Fault Condition: Logic "0" output
5	VCCR	RX Power Supply	N/C	Provide +5V DC through the recommended power supply filter circuit. Place the filter circuit as close as possible to the VCCR pin.
6	VCCT	TX Power Supply	N/C	Provide +5V DC through the recommended power supply filter circuit. Place the filter circuit as close as possible to the VCCT pin
7	TD-	TX Invert Data Input	PECL	
8	TD+	TX Data Input	PECL	
9	VEET	TX Ground	N/C	Directly connect this pin to transmitter signal ground plane.

Package Information

Unit: mm



Recommended Circuit



Application cautions

There are a few fundamental guidelines to follow when designing the transceiver circuit interface. On the board, every data connection should be an impedance match. The differential PECL data inputs and outputs line should be treaded as 50 ohm microstrip line, and vias should be avoided. The matching resistor should be placed at the end of each matched line. The signal detect (SD) output is PECL logic and must be loaded if it is to be used. The signal detect (SD) is relatively slow and not need 50 ohm termination (although it is capable of driving it). To reduce power, the signal detect output can be terminal with 510 ohm. Figure 6 shows the typical operating circuit for the module. The transceiver is high frequency, high bandwidth circuits. To ensure stability, use good high frequency layout techniques. Filter voltage supplies, and keep ground connections short. Use multiple vias where possible. Use 50 ohm microstrip line to connect the transceiver data inputs and outputs to other circuit.

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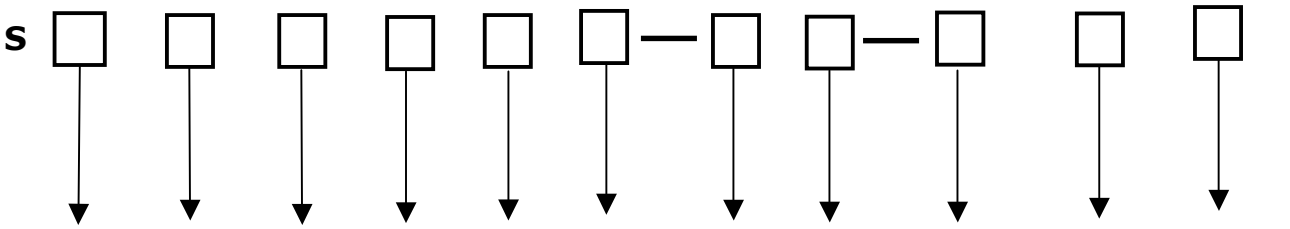

Part number	Product Information
SSTR5241-25-113	1550nm 1×9 622Mb/s 0~70℃