MICROSENS

4 port STM-16
TDM Multiplexer Module

Overview

4 port STM-16 TDM Multiplexer Module is a part of MICROSENS 10G Transport Platform, a high performance and flexible carrier-class transmission system. The 10G Transport Platform enables increasing transport capacities in CWDM, DWDM and SDH networks. The use of wide range TDM modules permits to reduce the number of necessary wavelengths and to decrease the overall cost of the application. Ethernet over SDH modules enable using existing SONET/SDH infrastructure for IP transmission.

The general features of the system:

- 19“ 2U Chassis with 5 module slots and management card
- Max. 5x single size modules i.e. 2x double size + 1x single size module
- Hot swappable modules & power supplies
- Redundant power supplies with -48 VDC input (opt. 230 VAC)
- Exchangeable air- and filter module
- Wide range of functional xWDM and TDM modules available

The functional modules of 10G Transport Platform include:

- TDM 8x GBE or 8x GFC to 10G/OC-192/STM-64
- TDM 5x GBE or 5x 2GFC to OC-192/STM-64
- TDM 4x OC-48/STM-16 to 10G/OC-192/STM-64
- TDM 2x GBE and 2x GFC to OC-48/STM-16
- 10G transponder with 3R, XFP and fixed Laser Versions
- 10G protocol converter 10G LAN to 10G WAN (OC-192/STM-64)
- DWDM MUX/DeMUX, OADMs, EDFAs

Introduction

MICROSENS 10G TDM STM-16 Module is a bidirectional Plug-in Board Unit offering the aggregation and transport of 4 telecom transparent services (OC 48/STM-16) onto a 10 Gb/s G709 OTU2 signal.

Features

- Four STM-16/OC-48 client port interfaces
- SFP modules for client port physical interfacing
- G709 OTU2 line format.
- FFI module 80 kms B&W and DWDM line interface
- DDM (Digital Diagnostic Monitoring) information from SFP and XFP/FFI

System description

MICROSENS 10G TDM STM-16 Module is a bi-directional device. It therefore has different sections:

- Upstream Section: from four STM-16/OC-48 optical inputs to G709 OTU2 optical output
- Downstream Section: from G709 OTU2 optical input to four STM-16/OC-48 optical outputs
- Common sections composed of :
    - Controller block, providing interfacing to the controller board hosting the SNMP Agent.
    - Power supplies: generates different internal power supplies from the -48V of the backplane
    - Front panel LEDs indicating the status of the ports, line and the device common functions

Upstream section

2.2.1 Input Ports interfacing

The upstream section has up to four optical inputs, which individually support STM 16/OC-48 (2.48832 Gb/s) input signal. Client Optical interfacing is done through standard SFP modules.

The following information is provided to the controller on a per port basis:

- SFP absence
- Loss of optical input signal
- Loss of Frame
- Out of Frame
- MS-AIS detected
- MS-RDI detected
- Non intrusive B1 BIP errors counting

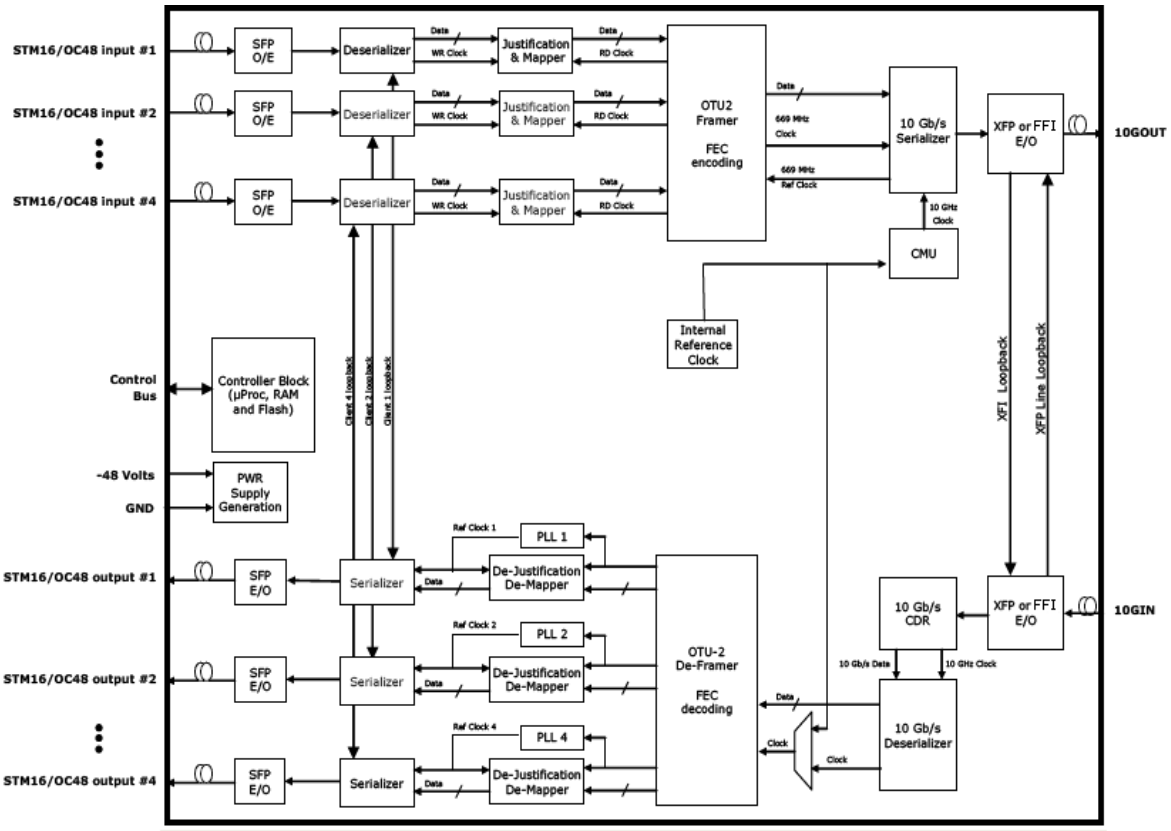

Figure 1: MS43065x Block diagram.

Mapper

Incoming signals must be synchronized and are mapped transparently in a proprietary frame prior of being multiplexed together for framing in a G.709 OTU2 signal. The organization of mapped client signals into the G.709 OTU2 is described on Figure 3. Synchronization of client signals is performed by a justification process.

For each OC-48/STM-16 signals, three different types of justification can be performed:

- Null Justification (0): the default mapping is used
- Negative Justification (-2): two data bytes are added to the default mapping.
- Positive Justification (+2): two data bytes are replaced by justification bytes in the default mapping.

Incoming STM-16/OC-48 signals frequency have a tolerance of ±20 ppm. Local system clocks have a tolerance of ±20 ppm.

The justification process ensures that the clock frequency of the STM16/OC48 data stream restored at the far end will be the one of the initial incoming STM16/OC48 signals (normally ±20 ppm).

The justification process is performed for each STM-16/OC-48 incoming signal in each G.709 OTU2 frame.

Synchronized STM-16/OC-48 incoming signals are mapped in a proprietary frame.

This frame transports the following information in addition to the data:

- Client Signal Fail indication: a bit in the mapping frame is set in case one of the following conditions are present on the incoming signal (see Figure 2)
- SFP not present
- Loss of incoming signal.
- Loss of Frame
- Out of Frame
- Justification buffer overflow
- MS-AIS detected

All these contributors to client signal fail are configurable through the SNMP agent.

- A client BIP-8 parity (CBIP) is computed over each mapped client signal and inserted in the corresponding mapping frame. The client BIP parity covers one line for each client signal (see Figure 3 for the organization of client signals in the outgoing G.709 OTU2 frame), which means the total number of bytes covered is 3792 bytes per mapped client signal (including the CBIP byte itself).

The following information is provided to the controller on a per port basis:

- Client Signal Fail asserted

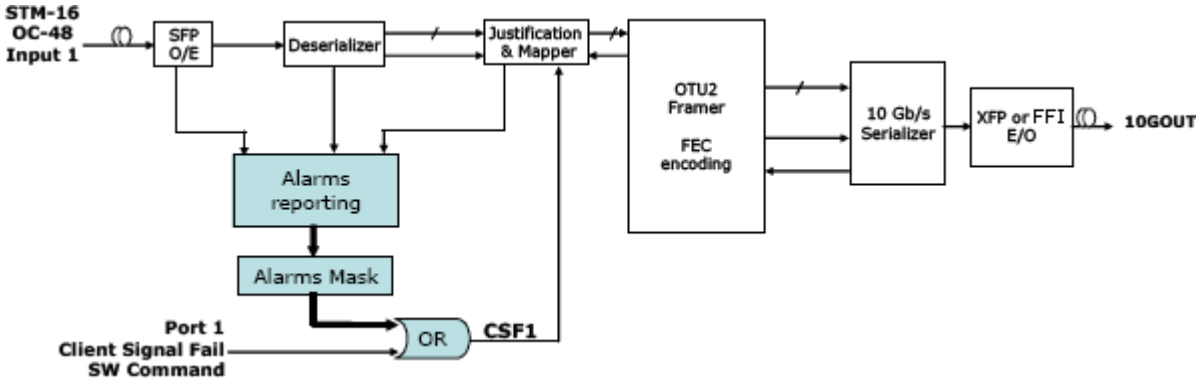

Figure 1: Upstream Client Signal Fail assertion principle.

Framer

Each of the mapped signals are multiplexed together and framed in a G.709 OTU2 output signal. On versions there is no Forward Error Correction (FEC) processing performed. All the bytes of the FEC zone (columns 3824 to 4080, rows 1 to 4) are set to 0x0.

BIP8 Section Monitoring (row1, byte 9) is calculated and inserted in its corresponding location in the outgoing signal.

The following information is provided to the controller on a per port basis:

- ODU2 AIS inserted (test purposes). The ODU2 AIS is inserted using the STAT entry of the Path Monitoring field (Row 3, Column 12, Bits 5 to 7).

Proprietary FEC encoder
This option is only applicable to some versions. A proprietary FEC is encoded providing a coding gain of 3.5 dB for an output BER of 10-12.

G709 FEC encoder
This option is only applicable to some versions. The standard G709 FEC is encoded providing a coding gain of 4.5 dB for an output BER of 10-12.

Line Optical Interfacing
Line optical interfacing can be performed through either an XFP module, either an FFI module. FFI modules are MICROSENS designed optical interfaces which present the same optical connector, as well as same management information as an XFP. FFI module provides 80 kms B&W or DWDM interface.

As opposed to XFP, FFI units are integrated in the MS43065xM and therefore cannot be removed separately.

The following alarms can be read from the Line Optical Interface:

- XFP absent
- Transmitter fault
- Transmitter CDR not locked
- Transmitter not ready

The following controls can be sent to the XFP/FFI:

- Shut down optical transmitter
- XFI loop-back (if implemented in XFP/FFI)
- XFP Line loop-back (if implemented in XFP/FFI)

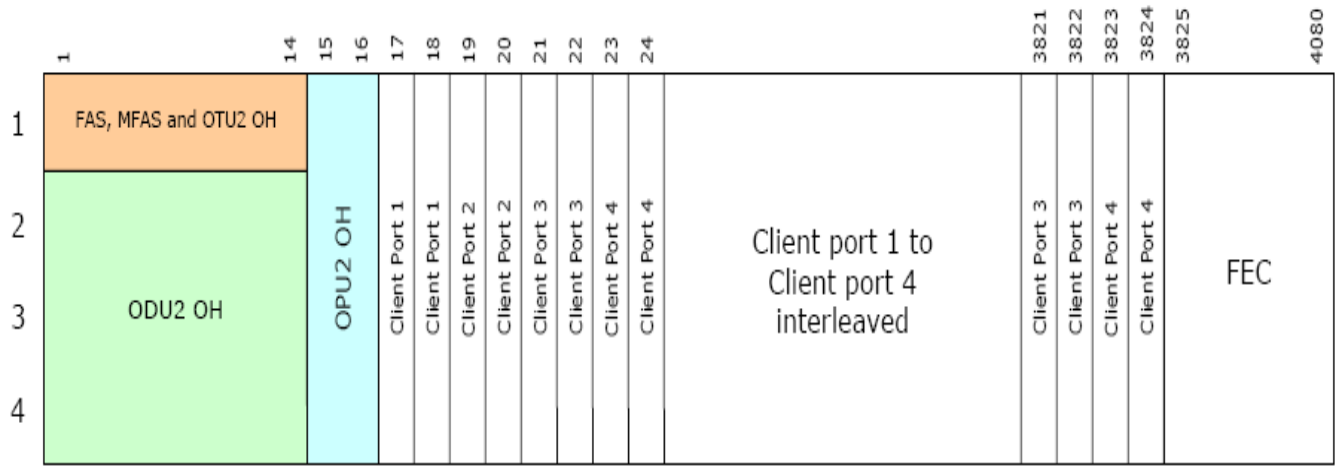

Figure 3: Organization of the mapped 4 client signals in G709 OTU2 frame.

DownStream Section

Line Optical Interfacing

Line optical interfacing can be performed through either an XFP module, either an FFI module. FFI modules are MICROSENS designed optical interfaces which present the same optical connector, as well as same management information as an XFP. FFI module provides 80 kms B&W or DWDM interface. As opposed to XFP, FFI units are not pluggable into the MS43065xM.

The following alarms can be read from the Line Optical Interface:

- XFP absent
- Loss of input signal
- Receiver CDR not locked
- Receiver not ready

De-Framer

G.709 OTU2 signal is received from the line optical interface.
G.709 OTU2 frame alignment is performed.

On versions there is no Forward error correction (FEC) decoder. The FEC zone is discarded in the De-Framer block. On another versions, FEC decoding is provided (see next sections)

BIP8 Section Monitoring parity calculation is computed. When an FEC decoder is provided, BIP8 parity calculation is the result of errors counted after correction. In that case a counter is provided for indicating the number of errors before correction.

G.709 OTU2 payload is de-multiplexed and the 4 channels are passed to the 4 Demapper blocks.

The following information is provided to the controller for the G.709 OTU2 incoming signal:

- Incoming Alignment Error on incoming signal
- ODU2-AIS received (Bit 5 to 7 of the STAT entry in the Path Monitoring field set to 1).
- BIP8 Section Monitoring errors counting
  The performance of the de-framer is:
- OOF to In Frame transition
  In Frame state is declared upon reception of two consecutive frames containing the framing pattern searched. Framing pattern searched is a 4 bytes pattern overlapping the OA1-OA2 transition.
- In Frame to OOF transition
  OOF state is declared upon reception of five consecutive frames not containing the framing pattern searched. Framing pattern searched is a 3 bytes pattern overlapping the OA1-OA2 transition.

IAE is declared upon 3 consecutive msec of OOF state.
IAE is reset upon 3 consecutive msec of In Frame state.

Proprietary FEC decoder

This option is only applicable to some versions. FEC is decoded and errored symbols are corrected. The coding gain provided by the FEC is 3.5 dB for an output BER of 10-12.

The following information is provided to the controller for the G.709 OTU2 incoming signal:

- Number of corrected errors counting
- Status indicating if there are uncorrected errors

G709 FEC decoder

This option is only applicable to some versions. FEC is decoded and errored symbols are corrected. The coding gain provided by the FEC is 4.5 dB for an output BER of 10-12.

The following information is provided to the controller for the G.709 OTU2 incoming signal:

- Number of errors counted before correction
- Status indicating if there are uncorrected errors

De-Mapper and de-justification

The de-mapper extracts STM-16/OC-48 data from the proprietary mapping frame. The de-justification process allows recovering the STM-16/OC-48 data stream mapped at the far end.

Each de-mapper has an associated PLL for regenerating the far end incoming clock frequency, based on the information received from the de-justification mechanism. Client Signal Fail information is also extracted and reported to the controller block (see Figure 4).

BIP-8 parity (CBIP) is computed over each individual received channel and compared to the received BIP-8. Error counting is performed and the result is reported to the controller block.

Under failure conditions, an output client AIS (CAIS) signal is inserted on the outgoing client port.

The alarms leading to assertion of client AIS are:

- Incoming Alignment Error on G.709 OTU2 input.
- ODU2-AIS received on the G.709 OTU2 input.
- Incoming CSF detected on individual channel
- De-justification buffer overload on individual channels

All these contributors to client signal fail are configurable through the SNMP agent. The client AIS signal is configurable to provide an optical output port shut down, or to no specific action taken. The CAIS mechanism is described on Figure 5.

The following information is provided to the controller on a per port basis:

- CSF received
- CBIP errors counting
- CAIS asserted
- De-justification buffer overload

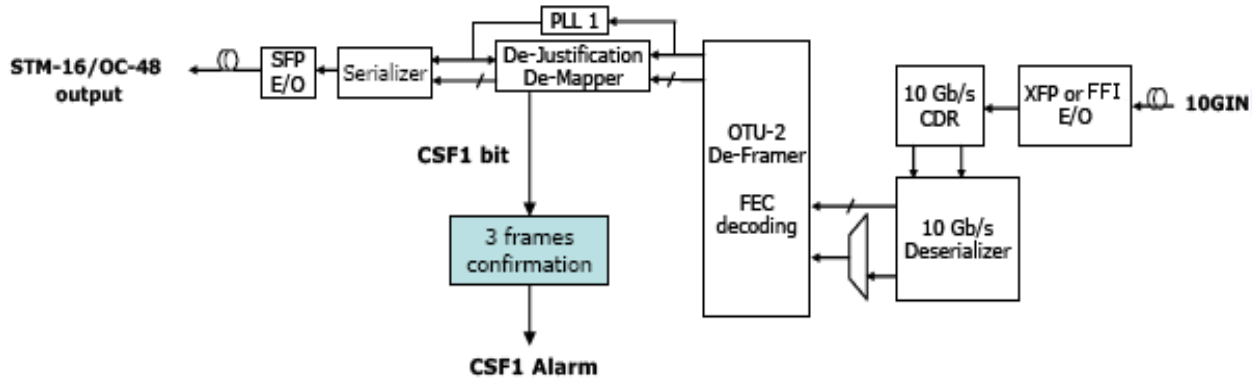

Figure 4: Downstream CSF detection mechanism.

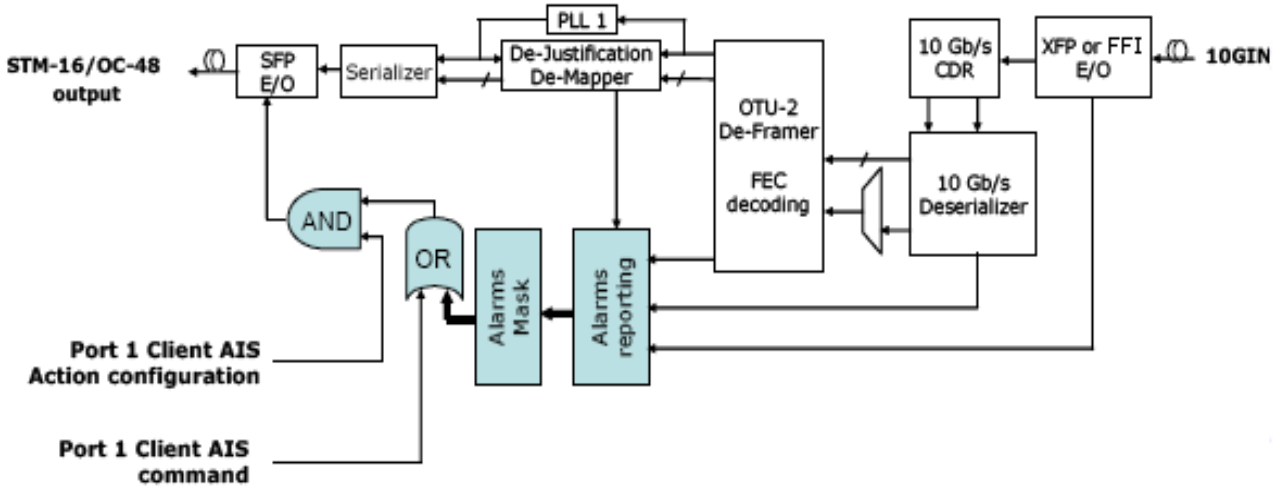

Figure 5: Downstream CSF mechanism.

Output port interfacing

Each channel is serialized and converted to an optical signal by SFP modules.
The following information is provided to the controller on a per port basis:

- Optical transmitter failure

The following configuration information is received from the controller block on a per port basis:

- Optical output shut-down

Maintenance Loop backs

Client loop back
As a test feature, an individual client loop back can be performed for maintenance operations. The client signal received on an input port is looped back on the corresponding outgoing client port. The description of the data path in case of client loop back is found on Figure 6.

XFI loop back (if supported)
As a test feature, an XFI loop back can be performed for maintenance operations, allowing looping back the transmitted 10Gb/s signal on the downstream section. The description of the data path in case of XFI loop back is found on Figure 7.

XFP Line loop back (if supported)
As a test feature, a line loop back can be performed for maintenance operation, allowing looping back the received 10 Gb/s signal on the upstream section. The clock and data path in case of XFP line loop back is described on Figure 8

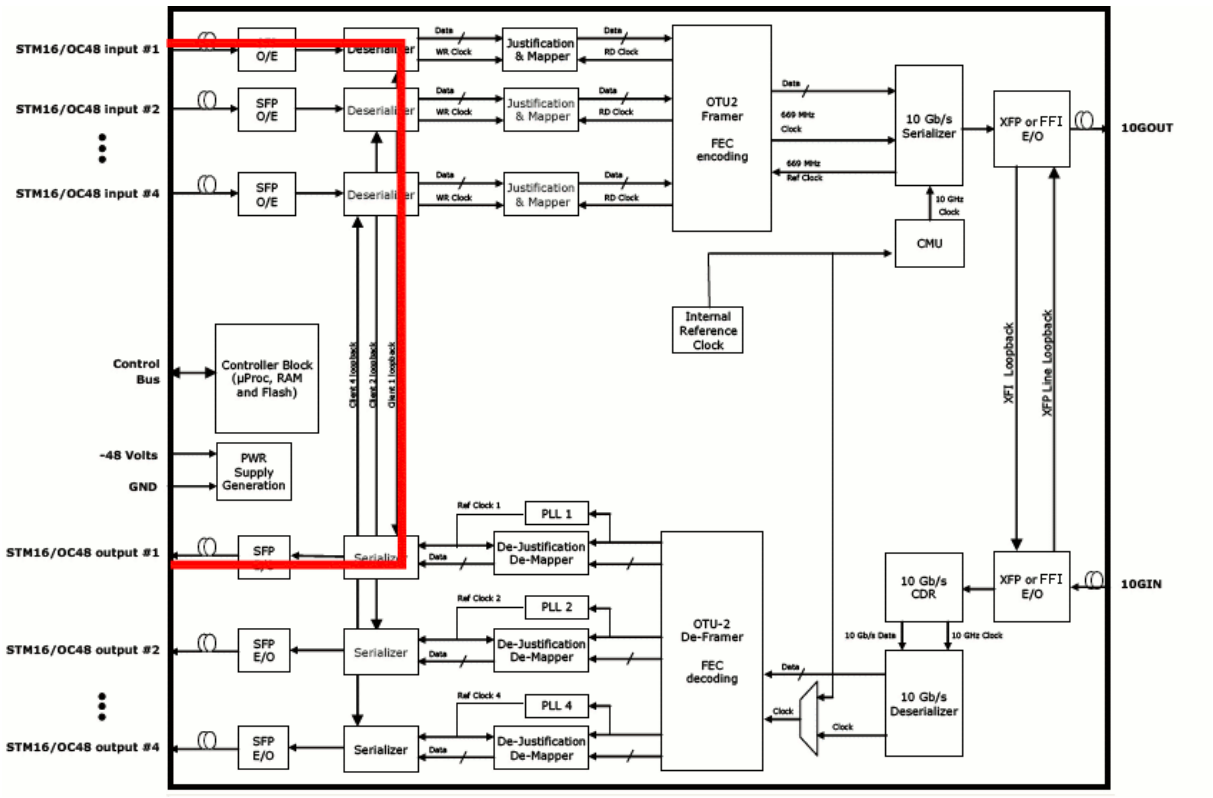

Figure 6: Signal data path in client loop-back operation.

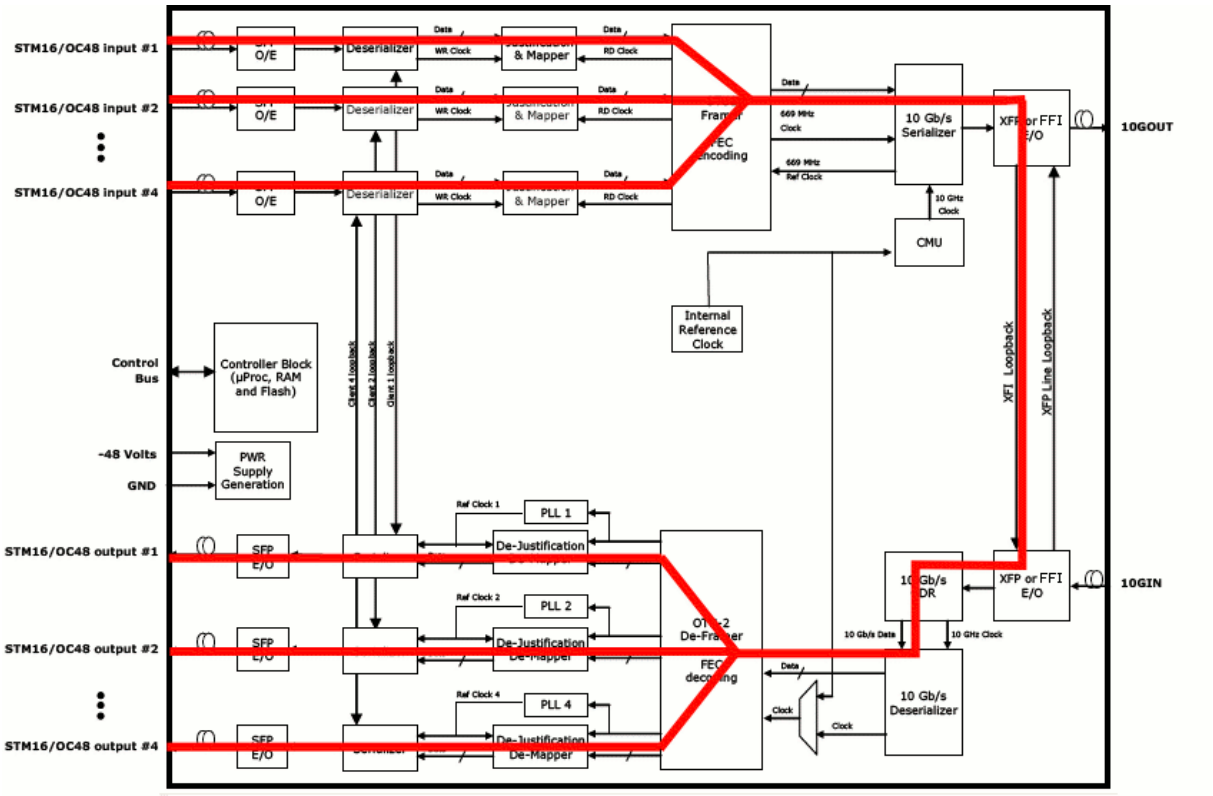

Figure 7: Signal data path in XFI loop-back operation.

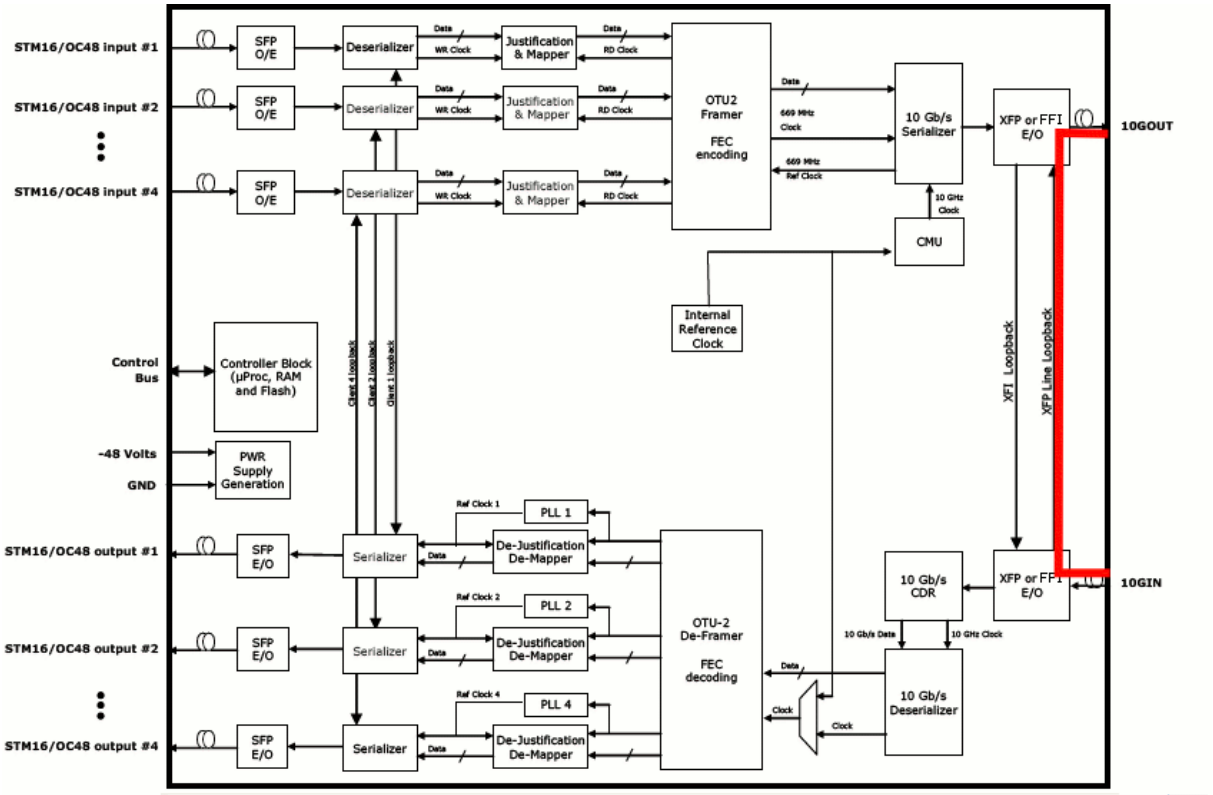

Figure 8: Signal data path in XFP line loop-back operation.

Clock Generation Unit

UpStream Clock Generation Unit

The UpStream Clock generation unit generates all internal clock signals required by the upstream part of the MS43065xM. The reference clock is internal to the MS43065xM and has a stability of +/- 20 ppm.

The following information is made available to the controller block:

- Upstream clock multiplier unit not locked

DownStream Clock Generation Unit

The DownStream Clock generation unit generates all internal clock signals required by the downstream part of the MS43065xM. Under normal operation, this block is driven by the recovered clock from the incoming 10 Gb/s signal. In case of failure of the incoming signal, this block is driven by the MS43065xM upstream reference clock.

The following information is made available to the controller block:

- DownStream clock recovery unit not locked

Controller Block

The controller block is composed of a microprocessor associated with Flash and RAM memories. The controller block collects information from different functional blocks and configures the HW according to a configuration file received. The raw information (alarms, monitoring, inventory …) generated by the HW are processed by the microprocessor and delivered to the Management Board as high level consolidated data.

Power Supplies

The power supply block generates from the received external -48 volts, the different internal supplies needed.

Interface Specifications

Client Interfaces Optical Characteristics

Client interfaces are provided by SFP transceivers. The optical characteristics are therefore given in the data sheet of the SFPs plugged into the MICROSENS module.

MS430650M and MS430651M Line Interface characteristics

Line optical interfacing is provided by XFP transceivers. The optical characteristics are therefore given in the data sheet of the XFPs plugged into the MICROSENS module.

MS430654M Line Interface characteristics

The MS430654M provides an 80 kms B&W or DWDM optical interfacing with the characteristics given in the following table:

General	Value			Unit
	Min.	Typ.	Max.	
Bit Rate nominal	10.70901	10.70922	10.70944	GHz
Line Coding		NRZ		-
Optical path max attenuation	-	-	21	dB
Optical path min attenuation	-	11	-	dB
Max path penalty @1600ps/nm	-	-	2	dB
Transmitter		**Value**		**Unit**
B&W wavelength range	1530	-	1560	nm
DWDM Wavelength range (100 GHz grid)	1529.55	-	1563.05	nm
	191.8	-	196	THz
Centre wavelength tolerance (EOL) (opt. B)	- 100	-	+ 100	pm
	- 12.5	-	+ 12.5	GHz
SMSR	30	-	-	dB
Pout (average value)	-2	-	+2	dBm
Extinction Ratio	10	-	-	dB
Receiver		**Value**		**Unit**
Wavelength Range	1525	-	1570	nm
Pin_{max} (BER @ 10^{-12}, average value, ER=10dB)	-	-9	-	dBm
Pin_{min} (sensitivity for BER @ 10^{-12}, average value, ER=10dB)	-	-25	-23	dBm
Receiver Reflectance			-27	dB

The following table gives the MS430654M wavelength plan:

Channel #	Optical Output Frequency (THz)	Optical Output Wavelength (nm)
-60	196,0	1529.55
-59	195,9	1530.33
-58	195,8	1531.12
-57	195,7	1531.90
-56	195,6	1532.68
-55	195,5	1533.47
-54	195,4	1534.25
-53	195,3	1535.04
-52	195,2	1535.82
-51	195,1	1536.61
-50	195,0	1537.40
-49	194,9	1538.19
-48	194,8	1538.98
-47	194,7	1539.77
-46	194,6	1540.56
-45	194,5	1541.35
-44	194,4	1542.14
-43	194,3	1542.94
-42	194,2	1543.73
-41	194,1	1544.53
-40	194,0	1545.32
-39	193,9	1546.12
-38	193,8	1546.92
-37	193,7	1547.72
-36	193,6	1548.51
-35	193,5	1549.32
-34	193,4	1550.12
-33	193,3	1550.92
-32	193,2	1551.72
-31	193,1	1552.52
-30	193,0	1553.33
-29	192,9	1554.13
-28	192,8	1554.94
-27	192,7	1555.75
-26	192,6	1556.55
-25	192,5	1557.36
-24	192,4	1558.17
-23	192,3	1558.98
-22	192,2	1559.79
-21	192,1	1560.61
-20	192,0	1561.42
-19	191,9	1562.23
-18	191,8	1563.05

Front Panel Layout

The TDM Multiplexer module occupies two slots in the MICROSENS chassis.

MS430650M
Line and Clients are XFP and SFP cages capable of hosting standard XFP/SFP modules.

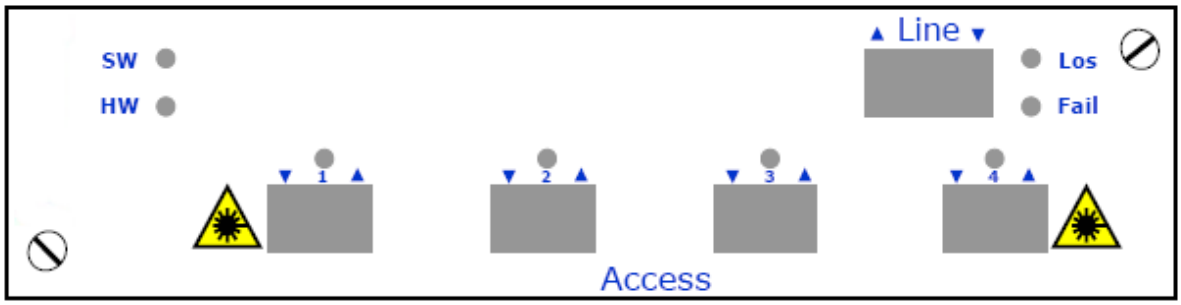

Figure 9: MS430650M and MS430651M front panel layout.

MS430654M
Line is a dual LC connector mounted on the TDM Multiplexer front panel. Clients are SFP cages capable of hosting standard SFP modules.

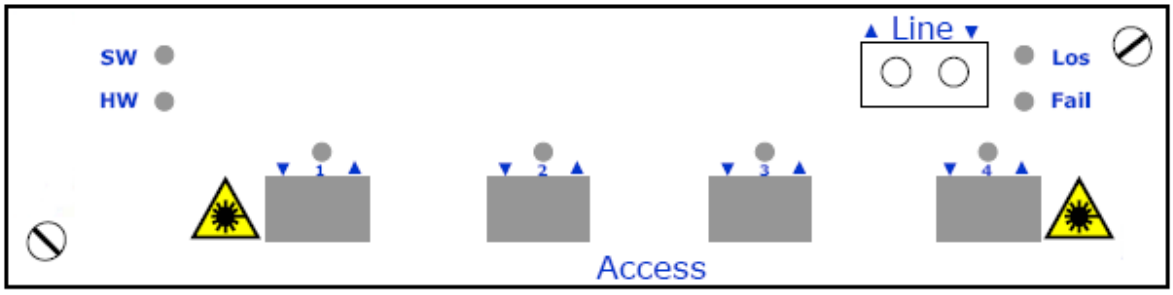

Figure 10: MS430654M front panel layout.

Technical Specifications

Type	4 port STM-16 TDM Multiplexer Module	
Connectors	XFP ports or FFI ports	
Data rate	9.953 Gbps, 10.3125 Gbps, 10.709 Gbps	
LED displays	*SW*	Software loading
	HW	Hardware ready
	Los	Signal lost
	Fail	Transmission failure
Power consumption	24 W typical	
Operating temperature	0°C to 50°C	
Storage temperature	-20°C to 70°C	

Order Information

Art. No.	Description	Connectors
MS430650M	TDM Unit 4x STM-16 over 10G, Line Port: XFP Slot (SFPs/XFP not included)	
MS430651M	TDM Unit 4x STM-16 over 10G with Line Protection, Line Port: XFP Slot (SFPs/XFP not included)	
MS430654M-x	TDM Unit 4x STM-16 over 10G, Line Port: FFI B&W (SFPs/FFI not included), x- FFI option	
MS430654M-x-nn	TDM Unit 4x STM-16 over 10G, Line Port: FFI DWDM (SFPs/FFI not included), x- FFI option, nn: Channel #	
MS430654M-B-nn	TDM Unit 4x STM-16 over 10G, Line Port: FFI DWDM (SFPs/FFI not included), 40km DWDM, nn: Channel #	