Product Specification Sheet

OLCPXXTXL-CD10

RoHS Compliant 100Gb/s CFP4 LR4 10km Optical Transceiver

SHENZHEN OLINKPHOTONICS INC., LTD

Add:4/F. No.A14 Building, Silicon-Valley-Dynamics Industrial Park, Longhua Street, Baoan District, Shenzhen, China.
Tel: +86-755-27215326, E-mail: sales@olinkphotonics.com

Product Features

●Supports up to 112Gbps bit rates
●Duplex LC connector
●Hot pluggable
●Operating electrical serial data rate up to 27.952493Gbps
●4 parallel electrical serial interface
●Applicable for 10km SMF connection
●Low power consumption (Max: 8W)
●Digital Diagnostic Monitor Interface
●MDIO Communication Interface
●Compliant with 100GBASE-LR4 and OTU4
●Operating case temperature:
Commerical:0 to 70 °C

Applications

●Local Area Network(LAN)
●Wide Area Network(WAN)
●Switch to router interface
●ITU-T OTU4 OTL4.4

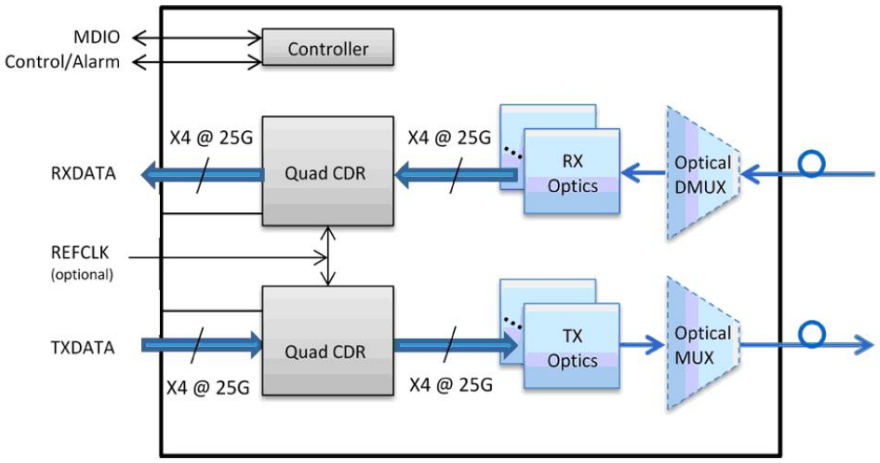
Standards

●Compliant with IEEE 802.3ba
●Compliant with CFP4 MSA hardware specifications
●Compliant with CFP4 MSA management specifications
●Compliant with ITU-T G709/Y.1331
●Compliant with RoHS

Functional Description

Olinkphotonics' OLCPXXTXL-CD10, 100G CFP4 LR4 optical transceiver integrates the transmit and receive path onto one module. On the transmit side, four lanes of serial data streams are recovered, retimed,and passed on to four laser drivers, which control four electric-absorption modulated lasers (EMLs) with 1296, 1300, 1305, and 1309 nm center wavelengths. The optical signals are then multiplexed into a single-mode fiber through an industry-standard LC connector.On the receive side, 4 lanes of optical data streams are optically demultiplexed by an integrated optical demultiplexer. Each data steam is recovered by a PIN photodetector and transimpedance amplifier, retimed, and passed on to an output driver. This module features a hot-pluggable electrical interface, low power consumption, and MDIO management interface.

Functional Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	Ts	-40	85	℃	
Relative Humidity	RH	0	85	%	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Data Rate	DR		103.2	112	Gb/s	
Supply Voltage	Vcc	3.14	3.3	3.46	V	
Operating Case Temp.	Tc	0		70	℃	

Electrical Characteristics

(Tested under recommended operating conditions,unless otherwise noted)

Parameter			Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics								
Supply Current	Tx Section		Icc	A			2	1
	Rx Section							
Power Supply Noise			Vrip				2% DC	1MHz
							3% 1	10MHz
Total Dissipation Power			Pw	W			8	
Low Power Mode Dissipation			Plow	W			2	
Inrush Current	Class1	and	I-inrush	mA/usec			100	
Turn-off Current	Class2		I-turnoff	mA/usec	-100			
Inrush Current	Class3	and	I-inrush	mA/usec			200	
Turn-off Current	Class4		I-turnoff	mA/usec	-200			
Different Signal Electrical Characteristics								
Single Ended Data Input Swing				mV	20		525	
Single Ended Data Output Swing				mV	180		385	

Differential Signal Output Resistance		Ω	80		120	
Differential Signal Input Resistance		Ω	80		120	
3.3V LVCMOS Electrical Characteristics						
Input High Voltage	3.3VIH	V	2.0		Vcc+0.3	
Input Low Voltage	3.3VIL	V	-0.3		0.8	
Input Leakage Current	3.3IIN	uA	-10		+10	
Output HighVoltage (IOH=100uA)	3.3VOH	V	Vcc-0.2			
Output Low Voltage (IOL=100uA)	3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	1.2VIH	V	0.84		1.5	
Input Low Voltage	1.2VIL V	0.3	1.2VIL V		0.36	
Input Leakage Current	1.2IIN	uA	-100		+100	
Output High Voltage	1.2VOH	V	1.0		1.5	
Output Low Voltage	1.2VOL	V	-0.3		0.2	
Output High Current	1.2IOH	mA			-4	
Output Low Current	1.2IOL	mA	+4			
Input Capacitance	Ci	pF			10	

High Speed Electrical Characteristics

Parameter	Symbol	Unit	Min.	Max.	Notes
Impedance	Zd	Ω	90	110	
Frequency		MHz	161.1328125		1/64 of electrical lane rate
Frequency Stability	△f	ppm	-100	100	For Ethernet
			-20	20	For Telecom
Differential Voltage	VDIFF	mV	400	900	Peak to Peak Differential
Common mode noise (rms)		mV		17.5	
RMS jitter		ps		10	Random Jitter Over frequency band of 10KHZ<f<10MHZ
Clock Duty Cycle		%	40	60	

Optical Characteristics

(Tested under recommended operating conditions,unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Optical Transmitter Characteristics						
Signaling rate, each lane		GBd	25.78125 ±100 ppm			100GBase-LR4
			27.9525 ±20 ppm			OTU4
Four Lane Wavelength Range	λ1	nm	1294.53	1295.56	1296.59	
	λ2		1299.02	1300.05	1301.09	
	λ3		1303.54	1304.58	1305.63	
	λ4		1308.09	1309.14	1310.19	
Total launch power		dBm			10.5	100GBase-LR4
					10	OTU4

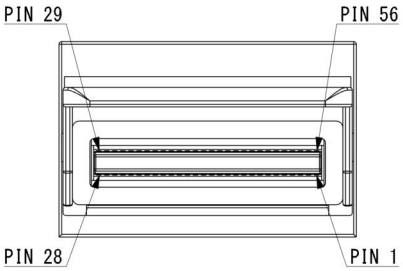
Average launch power, each lane	Pavg	dBm	-4.3		4.5	2
			-0.6		4	
Optical modulation amplitude, each lane (OMA)2	OMA	dBm	-1.3		4.5	
Difference in launch power between any two lanes (OMA)		dB			5	
Extinction ratio	ER	dB	4			100GBase-LR4
			4		6.5	OTU4
Side-mode suppression ratio	SMSR	dB	30			
Transmitter and dispersion penalty, each lane	TDP	dB			2.2	
Optical return loss tolerance		dB			20	
Transmitter reflectance3		dB			–12	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}			{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			100GBase-LR4
Optical Receiver Characteristics						
Receive Rate for Each Lane		Gbps		25.78125	27.9525	
Overload Input Optical Power	Pmax	dBm	5.5			3
Average Receive Power for Each Lane	Pin	dBm	-8.6		3	4
Receive Power In OMA for Each Lane	PinOMA	dBm			3	
Difference in Receive Power in OMA between Any Two Lanes		dBm				
Receiver Sensitivity in OMA for Each Lane	SOMA	dBm			-8.6	5
Stressed Receiver Sensitivity in OMA for Each Lane		dBm			-6.8	6,7

Notes:

1. The supply current includes CFP4 module's supply current and test board workingcurrent.
2. Average launch power, each lane (min) is informative for 100GBase-LR4, not the principal indicator of signal strength.
3. The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
5. Receiver sensitivity (OMA), each lane (max) is informative
6. Measured with conformance test signal at TP3 for BER=10-12
7. conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Pin Description

The CFP4 connector has 56 pins which are arranged in Top and Bottom rows. The pin map is shown in Table below:



	CFP4 Bottom		CFP4 Top
1	3.3V_GND	56	GND
2	3.3V_GND	55	TX3n
3	3.3V	54	TX3p
4	3.3V	53	GND
5	3.3V	52	TX2n
6	3.3V	51	TX2p
7	3.3V_GND	50	GND
8	3.3V_GND	49	TX1n
9	VND_IO_A	48	TX1p
10	VND_IO_B	47	GND
11	TX_DIS *(PRG_CNTL 1)*	46	TX0n
12	RX_LOS *(PRG_ALRM 1)*	45	TX0p
13	GLB_ALRMn	44	GND
14	MOD_LOPWR	43	*(REFCLKn)*
15	MOD_ABS	42	*(REFCLKp)*
16	MOD_RSTn	41	GND
17	MDC	40	RX3n
18	MDIO	39	RX3p
19	PRTADR0	38	GND
20	PRTADR1	37	RX2n
21	PRTADR2	36	RX2p
22	VND_IO_C	35	GND
23	VND_IO_D	34	RX1n
24	VND_IO_E	33	RX1p
25	GND	32	GND
26	*(MCLKn)*	31	RX0n
27	*(MCLKp)*	30	RX0p
28	GND	29	GND

Pin	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
3	3.3V			3.3V Module Supply Voltage
4	3.3V			3.3V Module Supply Voltage
5	3.3V			3.3V Module Supply Voltage
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS (PRG_CNTL1)	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALRM1)	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
14	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
16	MOD_RSTn	I	LVCMOS	Module Reset. "0" resets the module, "1" or NC =

			w/ PUR	module enabled, Pull Down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			
26	(MCLKn)			For optical waveform testing. Not for normal use.
27	(MCLKp)			For optical waveform testing. Not for normal use.
28	GND			
29	GND			
30	RX0p			25 Gbps receiver data; Lane 0
31	RX0n			25 Gbps receiver data bar; Lane 0
32	GND			
33	RX1p			25 Gbps receiver data; Lane 1
34	RX1n			25 Gbps receiver data bar; Lane 1
35	GND			
36	RX2p			25 Gbps receiver data; Lane 2
37	RX2n			25 Gbps receiver data bar; Lane 2
38	GND			
39	RX3p			25 Gbps receiver data; Lane 3
40	RX3n			25 Gbps receiver data bar; Lane 3
41	GND			
42	(REFCLKp)		CML	Module reference clock. No connect.
43	(REFCLKn)		CML	Module reference clock. No connect.
44	GND			
45	TX0p			25 Gbps transmitter data; Lane 0
46	TX0n			25 Gbps transmitter data bar; Lane 0
47	GND			
48	TX1p			25 Gbps transmitter data; Lane 0
49	TX1n			25 Gbps transmitter data bar; Lane 0
50	GND			
51	TX2p			25 Gbps transmitter data; Lane 0
52	TX2n			25 Gbps transmitter data bar; Lane 0
53	GND			
54	TX3p			25 Gbps transmitter data; Lane 3
55	TX3n			25 Gbps transmitter data bar; Lane 3
56	GND			

Hardware Control Pins

The CFP4 Module support real-time control functions via hardware pins, listed in the following

Pin	Symbol	Description	I/O	Logic	H	L	Pull-up/down
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS Low Power Enable Pull-Up	Low Power	Enable	Pull-Up Note1
16	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Notes:

1. Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP4 module
2. Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP4 module

Hardware Alarm Pins

The CFP4 Module supports alarm hardware pins listed in the following

Pin	Symbol	Description	I/O	Logic	H	L	Pull-up/down
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
20	RX_LOS	Receiver Loss of Signa	O	3.3V LVCMOS	Loss of Signal	OK	

Note:

1:.Pull-Down resistor (<100Ohm) is located within the CFP4 module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP4 Module supports alarm, control and monitor functions via an MDIO bus. The CFP4 MDIO pins are listed in the following:

.	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB-ALRMn	Global Alarm	I	3.3V LVCMOS	OK	Alarm	
18	MDIO	Management interface bidirectional data	I/O	1.2V LVCMOS			
17	MDC	Management interface clock input	I	1.2V LVCMOS			
19	PRTADR0	MDIO physical port address bit 0	I	1.2V LVCMOS	Per MDIO		
20	PRTADR1	MDIO physical port address bit 1	I	1.2V LVCMOS			
21	PRTADR2	MDIO physical port address bit 2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP4 hardware Signal Pins are listed in the following:

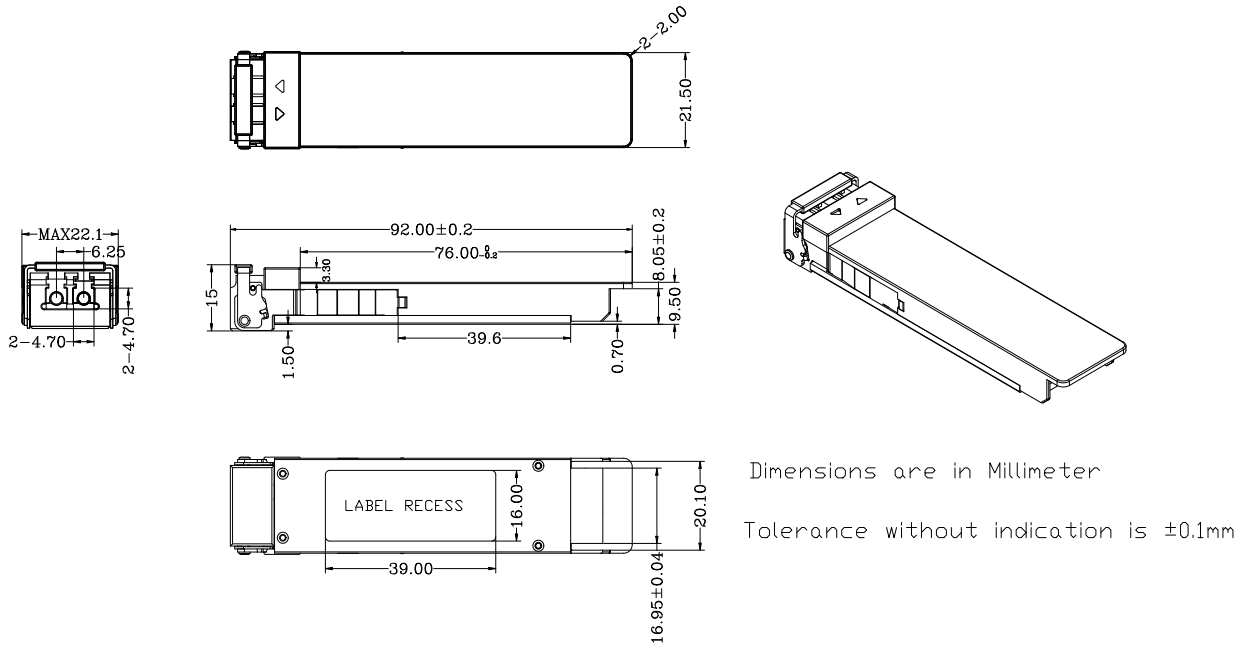
Parameter	Symbol	Unit	Min.	Max.	Notes
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert	ms		1	
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert	s		60	Stored in NVR register 8072h
Management interface clock period	t_prd	ns	250		MDC is 4 MHz rate or less
Host MDIO setup time	t_setup	ns	10		
Host MDIO hold time	t_hold	ns	10		
CFP4 MDIO delay time	t_delay	ns	0	175	
GLB_ALRM assert time	GLB_ALRMn_assert	ms		150	A logic “OR” of associated MDIO alarm and status registers
GLB_ALRM deassert time	GLB_ALRMn_deassert	ms		150	A logic “OR” of associated MDIO alarm and status registers
Minimum pulse width of control pin signal	t_CNTL	μs	100		
Initialization time from reset	t_initialize	s		2.5	
TX_Disable assert time	t_deassert	μs		100	Transmitter disable, application specific

TX_Disable deassert time1	t_assert	ms		5	Time from Tx Disable pin deasserted until CFP4 module enters the Tx-turn-on state Stored in NVR register 8073h
RX_LOS assert time	t_loss_assert	μs		100	From occurrence of loss of signal to assertion of RX_LOS
RX_LOS deassert time	t_loss_deassert	μs		100	From occurrence of return of signal to deassert of RX_LOS

CFP4 Lane Assignment

Lane	Center Frequency	Center Wavelength	Wavelength Range
L0	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L1	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L2	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L3	229.0 THz	1309.14 nm	1308.09 to 1310.19 nm

Package Dimensions



Ordering Information

Part Number	Description
OLCPXXTXL-CD10	100G CFP4 LR4 10Km 0~70℃

For More Information

SHENZHEN OLINKPHOTONICS INC., LTD
Add:4/F. No.A14 Building, Silicon-Valley-Dynamics Industrial Park, Longhua Street, Baoan District, shenzhen
Tel: +86-755-27215326
Fax: +86-755-27217051
E-mail:sales@olinkphotonics.com
Website:www.olinkphotonics.com