Product Specification Sheet

OLSQXXTXL-CD10C

RoHS Compliant 100Gb/s QSFP28 CWDM4 10km Optical Transceiver

SHENZHEN OLINKPHOTONICS INC., LTD

Add:4/F. No.A14 Building, Silicon-Valley-Dynamics Industrial Park, Longhua Street, Baoan District, Shenzhen, China.
Tel: +86-755-27215326, E-mail: sales@olinkphotonics.com

Product Features

Duplex LC receptacle optical interface
Single +3.3V power supply
Hot-pluggable QSFP28 MSA form factor
4x25G Electrical Serial Interface
Compliant with 4x28G(CEI-28G-VSR)
AC coupling of CML signals
Transmitter: cooled 4x25Gb/s CWDM TOSA (1270，1290，1310，1330nm)
Receiver: 4x25Gb/s PIN ROSA
Low power dissipation(Max:3.5W)
Built in digital diagnostic function
Operating case temperature range:0℃ to 70℃
Compliant with 100GBASE-LR4
I2C Communication Interface

Applications

100GBASE-LR4
Infiniband QDR and DDR interconnects
100G Datacom connections

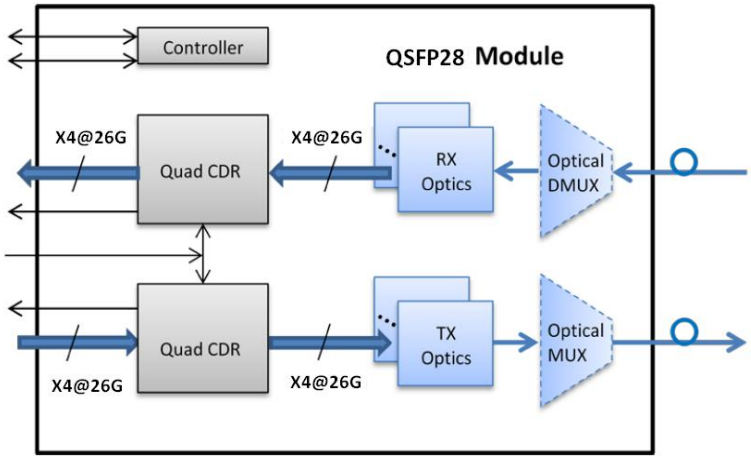
Standards

Compliant with IEEE 802.3ba
Compliant with QSFP28 MSA hardware specifications
Compliant with RoHS

Functional Description

The 100G QSFP28 LR4 optical transceiver integrates the transmit and receive path onto one module. On the transmit side, four lanes of serial data streams are recovered, retimed,and passed on to four laser drivers, which control four electric-absorption modulated lasers (CWDM) with 1270, 1290, 1310, and 13330 nm center wavelengths. The optical signals are then multiplexed into a single-mode fiber through an industry-standard LC connector.On the receive side, four lanes of optical data streams are optically demultiplexed by an integrated optical demultiplexer. Each data steam is recovered by a PIN photodetector and transimpedance amplifier, retimed, and passed on to an output driver. This module features a hot-pluggable electrical interface, low power consumption, and 2-wire serial interface.

Functional Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	Ts	-40	85	℃	
Relative Humidity	RH	0	85	%	
Rx Damage Threshold,per Lane	PRdmg	5.5		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit	Note
Data Rate	DR		103.1		Gb/s	
Supply Voltage	Vcc	3.14	3.3	3.47	V	
Supply Current	Icc			1.06	A	
Operating Case Temp.	Tc	0		70	℃	

Electrical Characteristics (T_{op}=0~70℃, Vcc=3.14~3.47V)

(Tested under recommended operating conditions,unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Signaling rate per lane	DRPL	25.78125 ± 100 ppm			Gb/s	
Differential input return loss (min)	RLd(f)	9.5 – 0.37f, 0.01≤f<8 4.75 – 7.4log10(f/14), 8 ≤f<19			dB	
Differential to common mode input return loss (min)	RLdc(f)	22-20(f/25.78), 0.01≤f<12.89 15-6(f/25.78), 12.89≤f<19			dB	
Differential termination mismatch	Tm			10	%	
Eye width	Ew			0.46	UI	
Applied pk-pk sinusoidal jitter	Ppj	Per IEEE 802.3bm				
Eye height	Eh		95		mV	
DC common mode voltage	DCv	-350		2850	mV	
Receiver						
Signaling rate per lane	DRPL	25.78125 ± 100 ppm			Gb/s	
Differential data output swing	Vout,pp	400		800	mV	
Eye width	Ew	0.57			UI	
Vertical eye closure				5.5	dB	
Differential output return loss (min)	RLd(f)	9.5 – 0.37f, 0.01≤f<8 4.75 – 7.4log10(f/14), 8 ≤f<19			dB	
Common to differential mode conversion return loss (min)	RLdc(f)	22-20(f/25.78), 0.01≤f<12.89 15-6(f/25.78), 12.89≤f<19			dB	
Differential termination mismatch	Tm			10	%	
Transition time, 20% to 80%	Tr,Tf	12			ps	

Notes:

1.20%~80%

Optical Characteristics (Top=0~70℃, Vcc=3.14~3.47V)

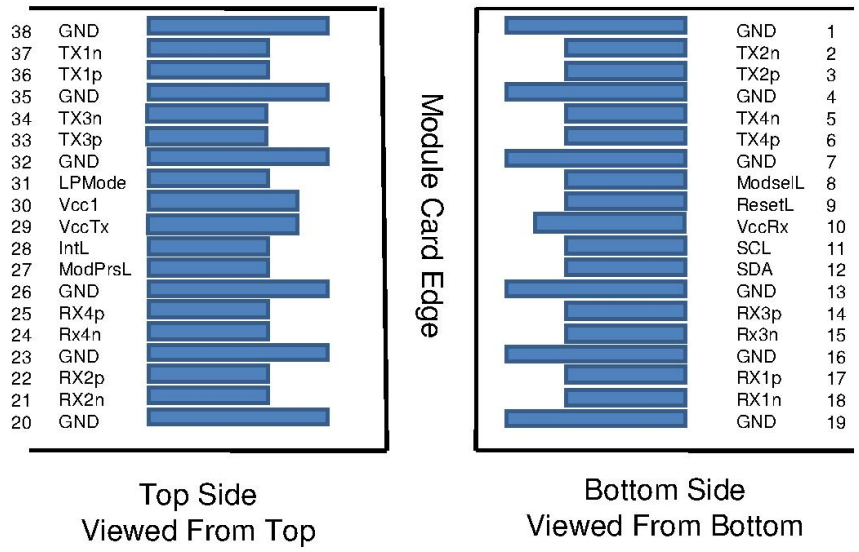
(Tested under recommended operating conditions,unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate, each lane		Gb/s	25.78125 ±100 ppm			1
Four Lane Wavelength Range	λ1	nm	1263	1270	1277	
	λ2		1283	1290	1297	
	λ3		1303	1310	1317	
	λ4		1323	1330	1337	
Total launch power	Pout	dBm			10.5	
Average launch power, each lane	Pavg	dBm	-4.5		2.5	2,7
Extinction ratio	ER	dB	4			
Side-mode suppression ratio	SMSR	dB	30			
Average launch power of OFF transmitter, per lane	POFF	dBm			-30	
Optical return loss tolerance		dB			20	
Transmitter reflectance		dB			–12	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}			{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			3
Receiver						
Receive Rate for Each Lane		Gb/s	25.78125 ±100 ppm			4
Four Lane Wavelength Range	λ1	nm	1263	1270	1277	
	λ2		1283	1290	1297	
	λ3		1303	1310	1317	
	λ4		1323	1330	1337	
Overload Input Optical Power	Pmax	dBm	5.5			
Average Receive Power for Each Lane	Pin	dBm	-11.2		2.5	5,7
Receiver Sensitivity(OMA)per lane	Psens1	dBm			-11.2	
Stressed Sensitivity(OMA) per lane	Psens2	dBm			-6.8	6
Return Loss	RL	dB	-26			
Receiver Electrical 3dB upper cutoff frequency, per lane		GHz			31	
Los De-Assert	Pd	dBm			-11.6	
Los Assert	Pa	dBm	-23.6			
Loss Hysteresis	Pd-Pa	dBm		2		

Notes:

1. Transmitter consists of 4 lasers operating at 25.78Gb/s each.
2. Minimum value is informative.
3. Hit ratio $5x10^{-5.}$
4. Receiver consists of 4 photodetectors operating at 25.78Gb/s each.
5. Minimum value is informative, equals min TxOMA with infinite ER and max channel insertion loss.
6. SRS is measured with vertical eye closure penalty of 1.8 dB max, J2 of 0.30 UI, and J9 of 0.47 UI.
7. Power value and power accuracy are with all channels on..

Pin Description



Pin	Name	Logic	Description	
1	GND		Ground	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	10
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	10
4	GND		Ground	1
5	Tx4n	CML-I	Transmitter Inverted Data Input	10
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	10
7	GND		Ground	1
8	ModSelL	LVTTL-I	Module Select	3
9	ResetL	LVTTL-I	Module Reset	4
10	Vcc Rx		+3.3V Power Supply Receiver	2
11	SCL	LVCMOS	2-wire serial interface clock	5
12	SDA	LVCMOS	2-wire serial interface data	5
13	GND		Ground	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	9
15	Rx3n	CML-O	Receiver Inverted Data Output	9
16	GND		Ground	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	9
18	Rx1n	CML-O	Receiver Inverted Data Output	9
19	GND		Ground	1
20	GND		Ground	1
21	Rx2n	CML-O	Receiver Inverted Data Output	9
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	9
23	GND		Ground	1
24	Rx4n	CML-O	Receiver Inverted Data Output	9
25	Rx4p	CML-O	Receiver Non-Inverted Data Output	9
26	GND		Ground	1
27	ModPrsL	LVTTL-O	Module Present	6
28	IntL	LVTTL-O	Interrupt	7

29	Vcc Tx		+3.3V Power supply transmitter	2
30	Vcc1		+3.3V Power supply	2
31	LPMode	LVTTL-I	Low Power Mode	8
32	GND		Ground	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	10
34	Tx3n	CML-I	Transmitter Inverted Data Input	10
35	GND		Ground	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data	
37	Tx1n	CML-I	Transmitter Inverted Data Input	10
38	GND		Ground	1

Notes:

1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA. Recommended host board power supply filtering is shown below .

3: The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4: The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5: Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1.

Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology.

6: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

7: IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

8: The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control

used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

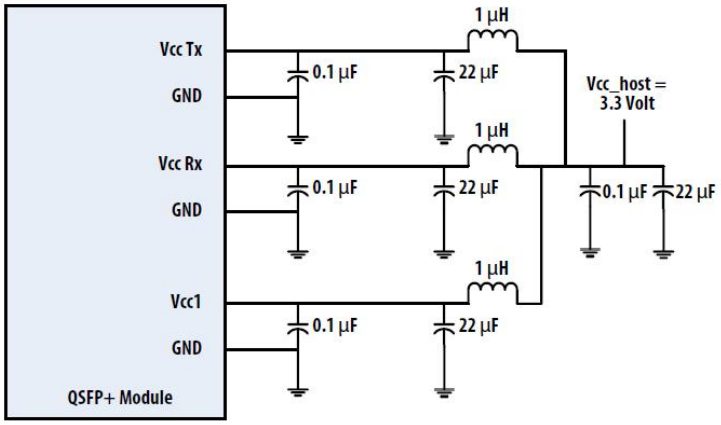
9: Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards.

Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host

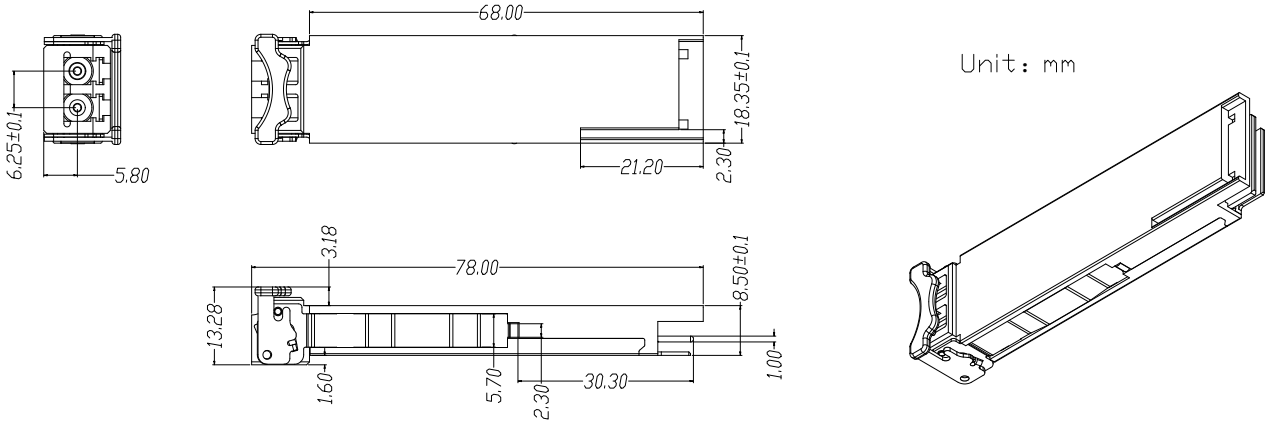
designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential. Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

10: Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards. Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential. Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended. In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to SFF- 8636.

Recommended Power Supply Filter



Package Dimensions



Ordering Information

Part Number	Description
OLSQXXTXL-CD10C	QSFP28 CWDM4 10km, 0~70℃, with Digital Diagnostic Monitor, Low power

For More Information

SHENZHEN OLINKPHOTONICS INC., LTD
Add:4/F. No.A14 Building, Silicon-Valley-Dynamics Industrial Park, Longhua Street, Baoan District, shenzhen
Tel: +86-755-27215326
Fax: +86-755-27217051
E-mail:sales@olinkphotonics.com
Website:www.olinkphotonics.com