Features

- Receiver unit with InGaAs PIN photodiode
- Meet SFF MSA and SFP-8472 with single LC receptacle
- Operating data rate up to 2.5Gbps
- Digital diagnostic monitoring
- Hot-pluggable
- Metal enclosure for lower EMI
- +3.3V Single power supply
- Operating temperature:0 to +70℃
- Qualified to meet the intent of Bellcore reliability practices
- CML logic simplifies interface to external circuitry
- LVTTL logic Signal level RX LOS
- Compliant ROHS and lead free
- With pull de-latch

Application

- Metro Access Rings and Point-to-point networking for SONET
- Gigabit Ethernet and Fibre Channel

General Description

The optical receiver is compliant with the Small Form- Factor Pluggable (SFP) Multi-Source Agreement (MSA) and SFP-8472. It is a high performance, costeffective module for serial optical data communication applications.

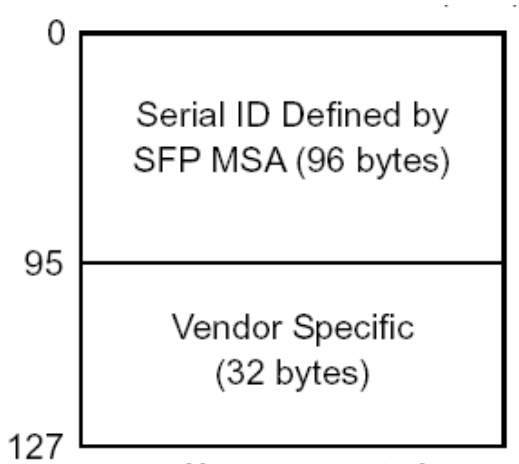
The receiver uses a hermetic packaged front end receiver (InGaAs PIN and preamplifier). The postamplifier is ac coupled to preamplifier through a capacitor and a low pass filter. The capacitor and LPF are enough to pass the signal from 5Mb/s to 2600Mb/s without significant distortion or performance penalty. The LPF limits the preamplifier bandwidth to improve receiver sensitivity. As the input optical is decreased, LOS will switch from low to high. As the input optical power is increased from very low levels, LOS will switch back from high to low.

EEPROM Section

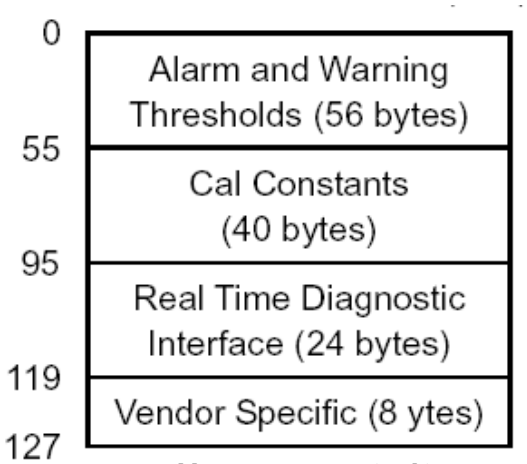
The optical receiver contains an EEPROM. It provides access to sophisticated identification information that describes the receiver's capabilities, standard interfaces, manufacturer, and other information.
The serial interface uses the 2-wire serial CMOS EEPROM protocol defined for the ATMEL AT24C01A/02/04 family of components. When the serial protocol is activated, the host generates the serial clock signal (SCL, Mod Def 1). The positive edge clocks data into those segments of the EEPROM that are not write protected within the SFP transceiver. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

The Module provides diagnostic information about the present operating conditions. The receiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture. Received power monitoring, supply voltage monitoring and temperature monitoring all are implemented. The diagnostic data are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at wire serial bus address A2h. The digital diagnostic memory map specific data field define as following.

Memory Map:



2 wire address 1010000x (A0h)



2 wire address 1010001x (A2h)

Performance Specifications

Table1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-40	+85	℃
Operating Temperature	To	0	+70	℃
Input Voltage	-	GND	Vcc	V
Power Supply Voltage	Vcc-Vee	-0.5	+3.6	V

Note: Stress in excess of maximum absolute ratings can cause permanent damage to the module

Table2. Operating Environment

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	+3.1	+3.5	V
Ambient Operating Temperature	TA	0	+70	℃

Table 3.Receiver optical-electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operate Wavelength	-	1260	-	1620	nm	-
Sensitivity	Pr	-	-	-18	dBm	2
Saturation	Ps	-3	-	-	dBm	2
LOS Asserted	-	-35	-	-	dBm	High Level: Alarm
LOS De-Assert	-	-	-	-18	dBm	
LOS Hysteresis	-	-	1.5	-	dB	
LOS LOW voltage	VLout	-	-	0.8	V	-
LOS HIGH voltage	VHout	2.0	-	-	V	-
Receiver Optical Return Loss	-	-	-	-27	dB	-
Power Supply Current	Icc	-	80	170	mA	1
Data Outputs Voltage	Vpp	400	800	1000	mV	-

Notes:

1. **The current excludes the output load current.**
2. **Minimum Sensitivity and saturation levels for a $2^{23}-1$ PRBS with 72 ones and 72 zeros inserted.**

Pin Definition

Pin Out Diagram

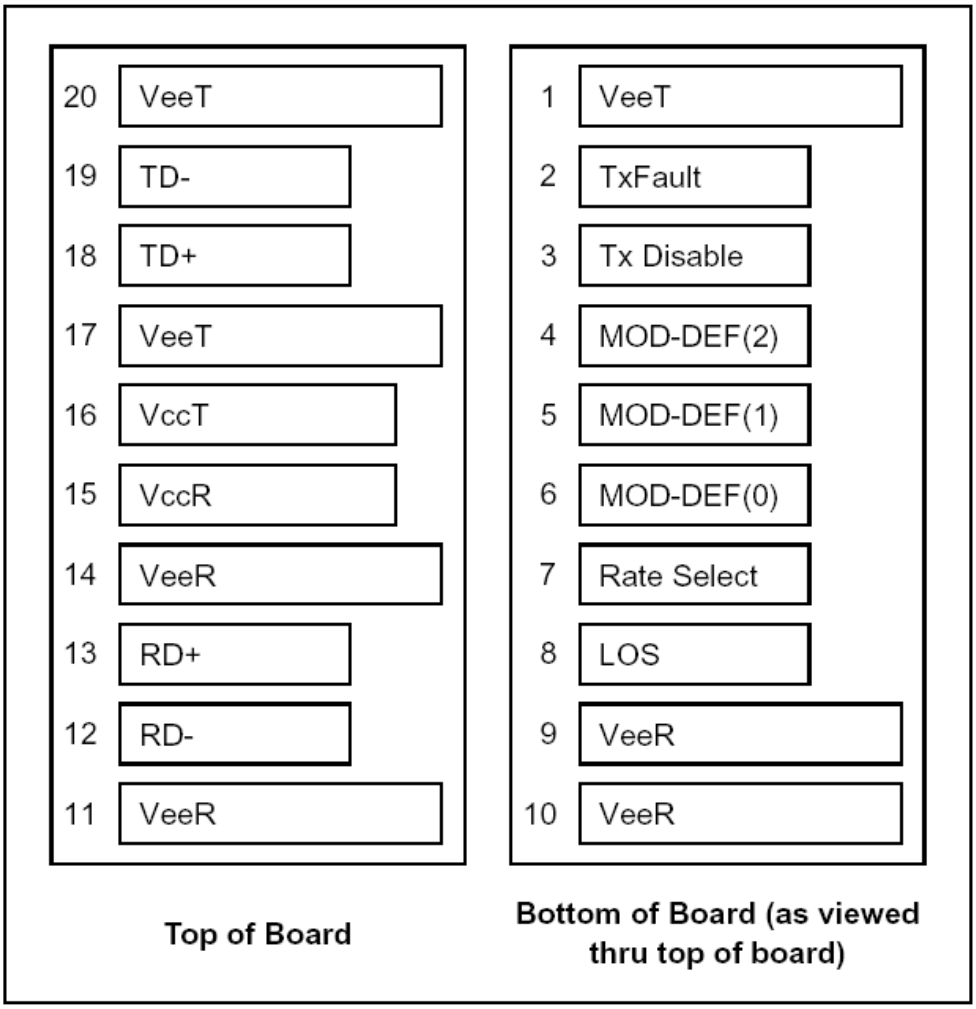


Table 4.Pin Function Definitions

Pin#	Name	Description	Notes
1	VeeT	Transmitter Ground	-
2	TX Fault	NC	-
3	TX Disable	NC	-
4	MOD-DEF2	Module Definition 2	Note 1, 2 wire serial ID interface
5	MOD-DEF1	Module Definition 1	Note 1, 2 wire serial ID interface
6	MOD-DEF0	Module Definition 0	Note 1, Grounded in Module
7	Rate Select	Not use	-
8	LOS	Loss of Signal	Notes 2
9	VeeR	Receiver Ground	Note 3
10	VeeR	Receiver Ground	Note 3
11	VeeR	Receiver Ground	Note 3
12	RD-	Inv. Received Data Out	Notes 4
13	RD+	Receiver Data out	Notes 4
14	VeeR	Receiver Ground	Note 3
15	VccR	Receiver Power	Note 5, 3.3V± 5%
16	VccT	Transmitter Power	Note 5, 3.3V± 5%
17	VeeT	Transmitter Ground	Note 3
18	TD+	NC	-
19	TD-	NC	-
20	VeeT	Transmitter Ground	Notes 3

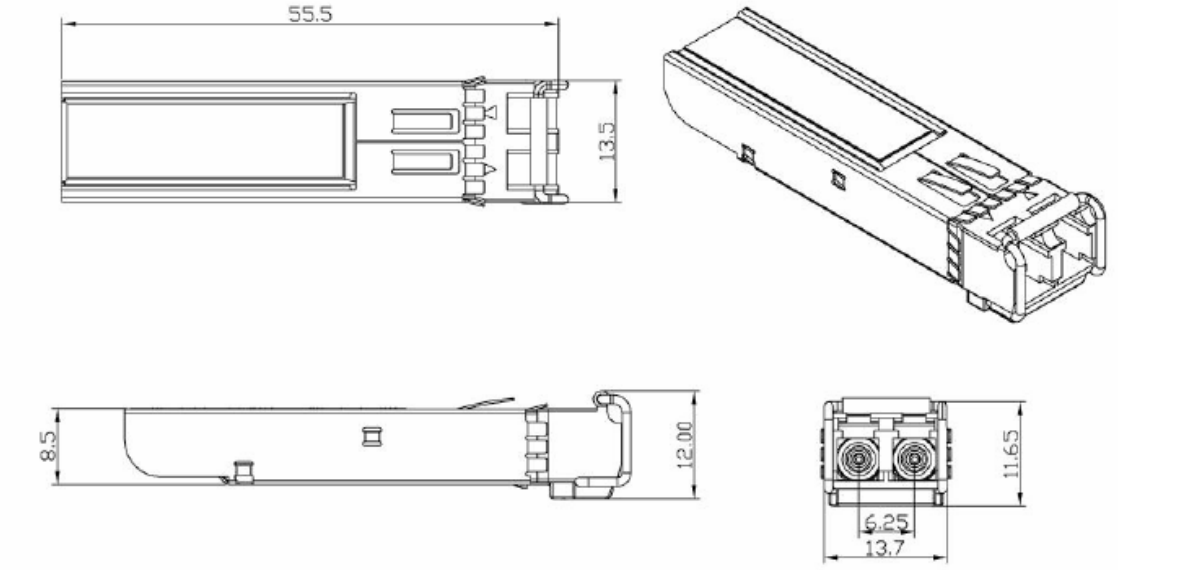
Note:

1. **Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7K – 10KΩ resistor on the host board. The pull-up voltage shall be VccT or VccR. Mod-Def 0 is grounded by the module to indicate that the module is present Mod-Def 1 is the clock line of two wire serial interface for serial ID Mod-Def 2 is the data line of two wire serial interface for serial ID**
2. **LOS (Loss of Signal) is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor. Pull up voltage between 2.0V and VccT, R+0.3V. When high, this output indicates the received optical power is below the worst-case receiver sensitivity(as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8V.**
3. **VeeR and VeeT may be internally connected within the SFP module.**
4. **RD-/+: These are the differential receiver outputs. They are AC coupled 100Ω differential lines which**

should be terminated with 100Ω (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board.

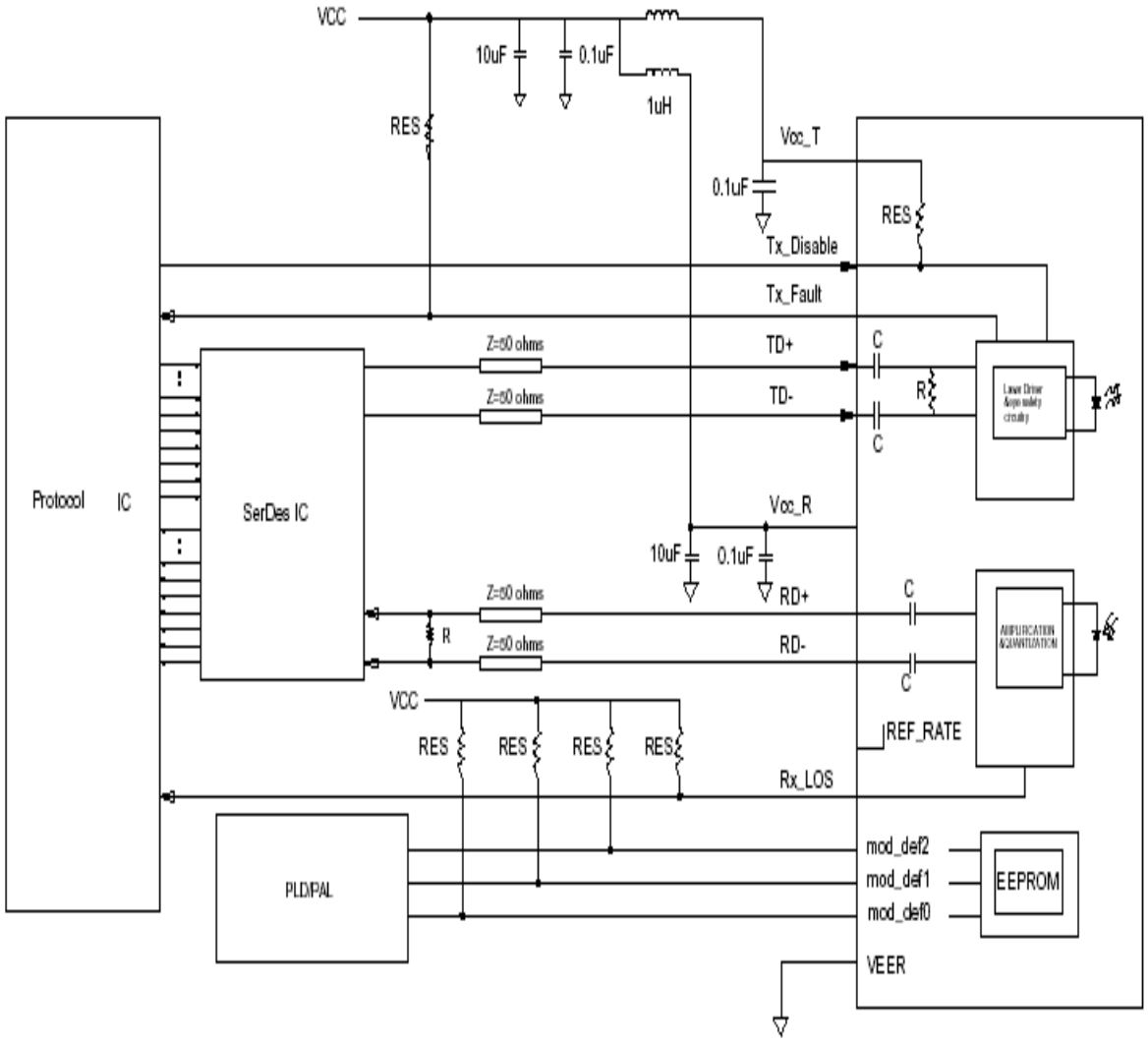
5. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3V ±5% at the SFP connector pin. Maximum supply current is 300mA. Recommended host board power supply filtering is shown below. Inductors with DC resistance of less than 1Ω should be used in order to maintain the required voltage at the SFP input pin with3.3V supply voltage. When the recommended supply filtering network is used, hotplugging of the SFP transceiver module will result in an inrush current of no more than 30 mA greater than the steady state value. VccR and VccT may be internally connected within the SFP transceiver module.

Package information



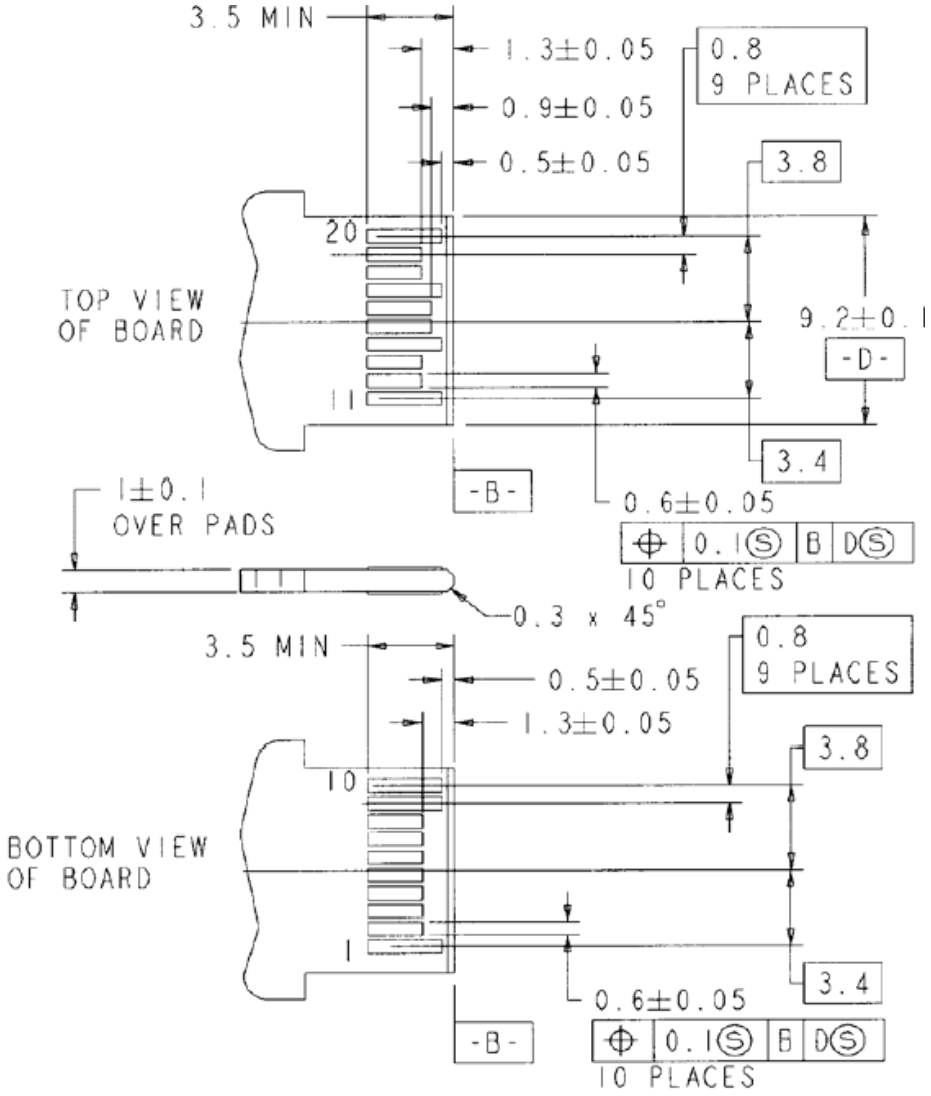
Unit: mm

Recommended Circuit



Note: 4.7K ohms < RES < 10K ohms

Recommended Board Layout Hole Pattern



For More Information

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Ordering Information

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Product classification
S: Normal
C: CWDM
M: Multi-mode

Package form:
P: SFP(W/DDM)
T: SFP(WO/DDM)

CWDM wavelength:
27:1270nm
29:1290nm
31:1310nm
33:1330nm
35:1350nm
37:1370nm
39:1390nm
41:1410nm
43:1430nm
45:1450nm
47: 1470nm
49: 1490nm
51: 1510nm
53: 1530nm
55: 1550nm
57: 1570nm
59: 1590nm
61: 1610nm

Data Rate:
3: 155M
4: 622M
5: 1.25G
6: 2.5G

LD/PD type:
F: FP/PIN
D: DFB/PIN
V: VCSEL/PIN
A: DFB/APD

Output Power

Operating Tempe Range:
1: 0～70℃
2: -40～85℃

Logic Level:
2: PECLSignle/TTLSD

Connector Type:
5: LC/PC

T: Transmitter
R: Receiver